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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 504362 KJR/lgl	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/NZ2004/000230	International filing date *(day/month/year)* 23 September 2004	Priority date *(day/month/year)* 24 September 2003

International Patent Classification (IPC) or national classification and IPC

Int. Cl.

B82B 3/00 (2006.01) ***H01L 21/26*** (2006.01) ***H01L 21/311*** (2006.01)
H01J 37/317 (2006.01) ***H01L 21/285*** (2006.01) ***H01L 21/3213*** (2006.01)

Applicant

NANOCLUSTER DEVICES LIMITED et al

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 3 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. [X] *(sent to the applicant and to the International Bureau)* a total of **6** sheets, as follows:
      - [ ] sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - [ ] sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. [ ] *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or table related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).
4. This report contains indications relating to the following items:

[X]	Box No. I	Basis of the report
[ ]	Box No. II	Priority
[ ]	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
[ ]	Box No. IV	Lack of unity of invention
[X]	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
[ ]	Box No. VI	Certain documents cited
[ ]	Box No. VII	Certain defects in the international application
[ ]	Box No. VIII	Certain observations on the international application

Date of submission of the demand 8 July 2005	Date of completion of this report 23 December 2005
Name and mailing address of the IPEA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized Officer **STEPHEN CLARK** Telephone No. (02) 6283 2781

Form PCT/IPEA/409 (Cover sheet) (April 2005)

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/NZ2004/000230

Box No. I Basis of the report

1. With regard to the **language**, this report is based on:

[X] The international application in the language in which it was filed

[ ] A translation of the international application into , which is the language of a translation furnished for the purposes of:

- [ ] international search (under Rules 12.3(a) and 23.1 (b))
- [ ] publication of the international application (under Rule 12.4(a))
- [ ] international preliminary examination (Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

[ ] the international application as originally filed/furnished

[X] the description:

pages **1,2,5-8,10-37** as originally filed/furnished
pages* **3,4,9** received by this Authority on **8 July 2005** with the letter of **8 July 2005**
pages* received by this Authority on with the letter of

[X] the claims:

pages **40-43,45** as originally filed/furnished
pages* as amended (together with any statement) under Article 19
pages* **38,39,44** received by this Authority on **8 July 2005** with the letter of **8 July 2005**
pages* received by this Authority on with the letter of

[X] the drawings:

pages **1-7** as originally filed/furnished
pages* received by this Authority on with the letter of
pages* received by this Authority on with the letter of

[ ] a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. [ ] The amendments have resulted in the cancellation of:

- [ ] the description, pages
- [ ] the claims, Nos.
- [ ] the drawings, sheets/figs
- [ ] the sequence listing *(specify)*:
- [ ] any table(s) related to the sequence listing *(specify)*:

4. [ ] This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

- [ ] the description, pages
- [ ] the claims, Nos.
- [ ] the drawings, sheets/figs
- [ ] the sequence listing *(specify)*:
- [ ] any table(s) related to the sequence listing *(specify)*:

If item 4 applies, some or all of those sheets may be marked "superseded."

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International application No.
PCT/NZ2004/000230

Box No. V **Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims 1-46	YES
	Claims	NO
Inventive step (IS)	Claims 1-46	YES
	Claims	NO
Industrial applicability (IA)	Claims 1-46	YES
	Claims	NO

2. Citations and explanations (Rule 70.7)

1. Muller et al., "Template-directed self-assembly of buried nanowires and the pearling instability"
2. TADA et al., "Channel waveguides fabricated in 2D photonic crystals of Si nanopillars"
3. US 6413880 Baski et al
4. PARTRIDGE et al., "Templated cluster assembly for production of metallic nanowires in passivated silicon V-grooves"

Novelty (N), Inventive Step (IS) Claims 1-46

None of citations 1-3 alone, or in obvious combination, disclose all of the features of any of the claims.

In particular, the accumulation of nanoparticles in, or against, the topographical feature being used as an etch mask was not found. The closest prior art was citation 2 above which had a similar accumulation of nanoparticles in, or against, a topographical feature, however the etching process forms a condensate around the nanoparticles which form the mask, rather than the nanoparticles themselves, also forming a mask thicker than the nanoparticle accumulation. It is not considered that the claimed invention would be obvious to a person skilled in the art, in light of this document.

Citation 4 was available on line on 14 March 2004, before the instant filing date, but after the instant priority date, and is thus a "P" category NPL document, that is not appropriate to be placed in Box VI. This document appears to be an identical disclosure to the instant specification, is by the instant inventors, and discloses all of the features of all of the claims.

- Development of the resist in order achieve the transfer of the pattern on the mask into the resist layer
- Etching so as to transfer the pattern into the substrate
- Removal of the remaining resist.

The chief limitation in this process is that the use of light to expose the resist limits the resolution that can be achieved, since light can usually only be focussed to a spot with diameter ~$\lambda/2$. Various alternative techniques have been used, including

- electron beam lithography[2], which can achieve high resolution but is inherently slow because it is a sequential write process
- nanoimprint lithography [3,4,5,6], which can achieve high resolution but is a relatively new technique that is unproven in industrial settings. Contact between a mold and the substrate may be disadvantageous since dust or other extraneous material can damage the mold or prevent pattern transfer.

OBJECT OF THE INVENTION

It is an object of the invention to provide a method of preparing nanoscale or up to micronscale patterns, particular wire-like structures on the surface of a substrate, and/or devices formed therefrom which overcome one or more of the abovementioned disadvantages, or which at least provide the public with a useful alternative.

SUMMARY OF THE INVENTION

According to a first aspect of the invention there is provided a **method of forming a pattern on or in a substrate surface** comprising or including the steps of:

a) Providing a substrate;
b) modifying the substrate surface to provide a topographical feature, or identifying a topographical feature on the substrate surface;
c) preparing a plurality of particles of size between about 0.5nm and 100 microns;
d) deposition of a plurality of the particles on the substrate surface in, or in the general vicinity of, the topographical feature;

e) formation of an arrangement of particles via accumulation of the particles, into or against or proximal to, the topographical feature;

f) removing at least a portion of the substrate by etching, the arrangement of particles acting as an etch mask.

Preferably the size of the particles is between about 0.5nm and 1000nm.

Preferably the substrate is at least partially an insulating or semiconducting material.

Preferably the pattern is in the form of a wire; the arrangement of particles being a substantially continuous chain of metallic clusters.

Preferably the wire is a nanowire and the particles are nanoparticles.

Preferably the modification includes formation of a step, depression or ridge in the substrate surface.

Preferably the modification comprises formation of a groove having a substantially v-shaped cross-section or inverted pyramid structure running substantially between the contacts.

Preferably the surface modification involves lithography.

Preferably the surface modification step involves the use of etching and takes advantage of the different etch rates of crystallographic planes in the substrate material.

Preferably the particles are composed of two or more atoms, which may or may not be of the same element.

iii. preparing a plurality of clusters;

iv. deposition of a plurality of the clusters on the substrate surface in, or in the general vicinity of, the topographical feature;

v. formation of an arrangement of clusters via accumulation of the clusters, into or against or proximal to, the topographical feature;

vi. subjecting the substrate and arrangement to an etching process, the arrangement of clusters acting as an etch mask

wherein either prior to or after step ii. one or more metallic or semiconducting layers are deposited on the substrate surface, such that the etching process removes substantially all of the one or more metallic or semiconducting layers other than the masked portion, and

wherein the process also includes, at any stage, a step of providing electrical contacts on the substrate so that once etching is complete a conducting pattern exists between the contacts; and

B. incorporating the contacts and wire into the device.

Preferably the device includes two or more contacts and the conducting pattern is a conducting wire.

Preferably the device is a nanoscale device, and the wire is a nanowire.

Preferably there is an additional step in A of removing the etch mask at some point following the etching process.

According to a further aspect of the invention there is provided a **device including or requiring a conduction path between two contacts formed on a substrate surface** prepared substantially according to the method described above.

CLAIMS:-

1. **A method of forming a pattern on or in a substrate surface** comprising or including the steps of:
   a) Providing a substrate;
   b) modifying the substrate surface to provide a topographical feature, or identifying a topographical feature on the substrate surface;
   c) preparing a plurality of particles of size between about 0.5nm and 100 microns;
   d) deposition of a plurality of the particles on the substrate surface in, or in the general vicinity of, the topographical feature;
   e) formation of an arrangement of particles via accumulation of the particles, into or against or proximal to, the topographical feature;
   f) removing at least a portion of the substrate by etching, the arrangement of particles acting as an etch mask.

2. A method as claimed in claim 1 wherein the size of the particles is between about 0.5nm and 1000 nm.

3. A method as claimed in claim 1 or 2 wherein the substrate is at least partially an insulating or semiconducting material.

4. A method as claimed in any one of the preceding claims wherein the pattern is in the form of a wire; the arrangement of particles being a substantially continuous chain of metallic clusters.

5. A method as claimed in claim 4 wherein the wire is a nanowire and the particles are nanoparticles.

6. A method as claimed in any one or more of the preceding claims wherein the modification includes formation of a step, depression or ridge in the substrate surface.

7. A method as claimed in claim 6 wherein the modification comprises formation of a groove having a substantially v-shaped cross-section or inverted pyramid structure running substantially between the contacts.

8. A method as claimed in claim 7 wherein the surface modification involves lithography.

9. A method as claimed in claim 8 wherein the surface modification step involves the use of etching and takes advantage of the different etch rates of crystallographic planes in the substrate material.

10. A method as claimed in any one of the preceding claims wherein the particles are composed of two or more atoms, which may or may not be of the same element.

11. A method as claimed in any one of the preceding claims wherein the accumulation of particles into or against or proximal to, the topographical feature relies upon the diffusion, sliding, bouncing or other movement of the particles across or on the surface of the substrate or any material deposited on the substrate.

12. A method as claimed in any one of the preceding claims wherein the substrate is substantially entirely an insulating or semiconductor material.

13. A method as claimed in claim 12 wherein the etching step removes substantially all of the substrate other than the masked portion thereby leaving a free-standing wire or bridge.

40. **A metallic or semi-conducting pattern on the surface of a substrate** prepared substantially according to method claimed in any one of claims 1 to 39.

41. **A method of fabricating a device including or requiring a conduction path between two contacts formed on a substrate surface,** comprising or including the steps of:

A. preparing a conducting pattern between two contacts according to a method comprising or including the steps of:

i. providing a semiconducting or insulating substrate;

ii. modifying the substrate surface to provide a topographical feature, or identifying a topographical feature on the substrate surface;

iii. preparing a plurality of clusters;

iv. deposition of a plurality of the clusters on the substrate surface in, or in the general vicinity of, the topographical feature;

v. formation of an arrangement of clusters via accumulation , of the clusters, into or against or proximal to, the topographical feature;

vi. subjecting the substrate and arrangement to an etching process, the arrangement of clusters acting as an etch mask

wherein either prior to or after step ii. one or more metallic or semiconducting layers are deposited on the substrate surface, such that the etching process removes substantially all of the one or more metallic or semiconducting layers other than the masked portion, and

wherein the process also includes, at any stage, a step of providing electrical contacts on the substrate so that once etching is complete a conducting pattern exists between the contacts; and

B. incorporating the contacts and wire into the device.

42. A method as claimed in claim 41 wherein the device includes two or more contacts and the conducting pattern is a conducting wire.

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